

LCFC Confidential

S360 ADA M/B Schematics Document

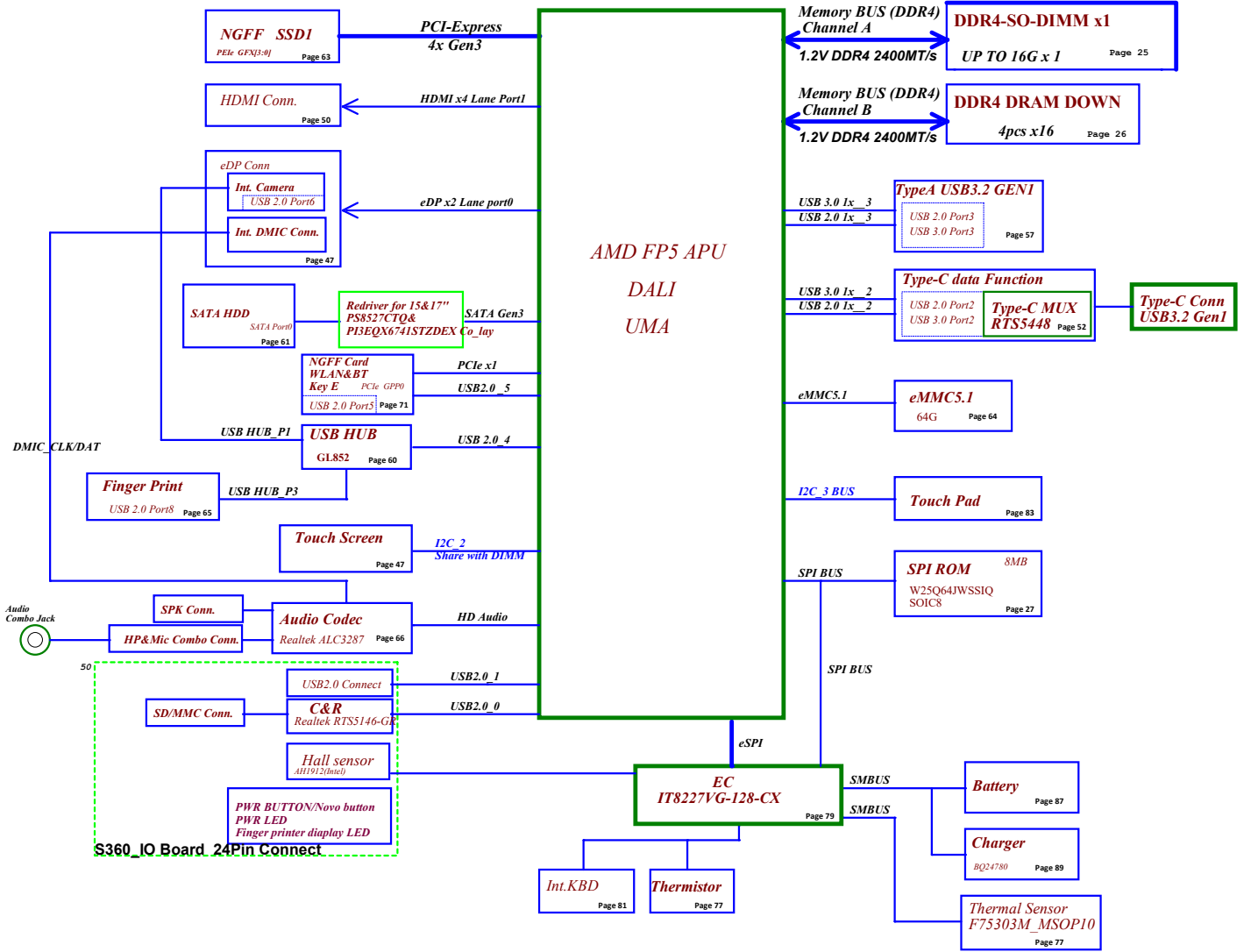
AMD FP5 DALI with DDR4


2020-11-30

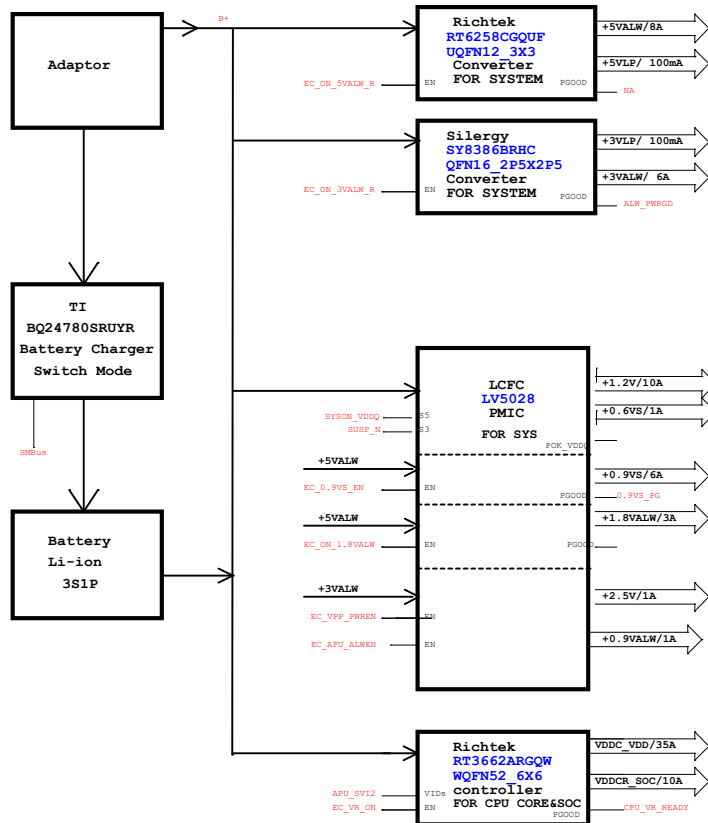
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S360 DALI M/B Schematics



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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+ +3VL +5VL	+3VALW +5VALW +3VALW_APU +1.8VALW +0.9VALW	+1.2V +2.5V	+5VS +3VS +1.8VS +0.8VS +0.6VS +VDDCR_CPU +VDDCR_SOC
S0	O	O	O	O
S0Ix				
S3	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

HSIO Matrix

HSIO PORT	Function
USB2.0	0 Cardreader
	1 USB (2.0) Port DB board
	2 TypeC Port
	3 TypeA 3.0 Port
	4 USB HUB
USB3.0	5 Bluetooth
	0 NC
	1 NC
	2 TypeC Port
Display	3 TypeA 3.0 Port
	0 eDP 2*lane
GFX	1 HDMI 1.4
	0
	1
	2 GFX x 4 SSD
	3
	4
	5 N/A
	6
GPP	7
	0 WLAN
	1 NC
	2 N/A
	3 N/A
	4 NC
	5 NC
	6 GPP x1 SATA HDD
	7 NC

BOM Structure Table

BOM Structure	BTO Item
@	Not Stuff
ME@	Connector
EMC@	EMC Part
EMC_NS@	EMC reserve Part
RF@	RF Part
RF_NS@	RF reserve Part
HDT@	HDT Debug part
REDRV@	Redriver part
NO17@	17' HDD Redriver reserve part
TS@	Touch Screen Part
17@	17' HDD Redriver part
NOTS@	Touch Screen reserve Part
FP@	Finger print Part
NOFP@	Finger print reserve Part

SMBUS Control Table OK

Source	EC IT8227C				CPU FPS DALI	
	EC_SMB_0 +3VS_APU	EC_SMB_1 +3VL_EC	EC_SMB_3 +3VS_EC	EC_SMB_4 +3V_MUX	I2C2/SMBus +3VS_APU	I2C3 +3VALW_APU
CPU	V SIC/SID					
Memory Down					V SMBus	
SODIMM						
BATT		V				
Charger		V				
WLAN						
PMIC			V			
Thermal Sensor	V					
TS					V	V Reserve
TP						V
Type-C MUX				V Only Read		

EC SMBus0 address

Device	Address
DGPU	
Thermal Sensor(NCT7718W)	
Thermal Sensor(F75303M_MSOP10)	0x4C
TOF	

EC SMBus1 address

Device	Address
Smart Battery	0x16
Charger	0x12

EC SMBus3 address

Device	Address
IMVP9	
PMIC (I2C)	0x34

EC SMBus4 address

Device	Address
Type-C MUX (RT5544B)	N/A

SMBus4 Only read TypeC Port current setting

PCH I2C2 address

Device	Address
CHA SO-DIMM	TBD
Touch Panel	0x10

PCH I2C3 address

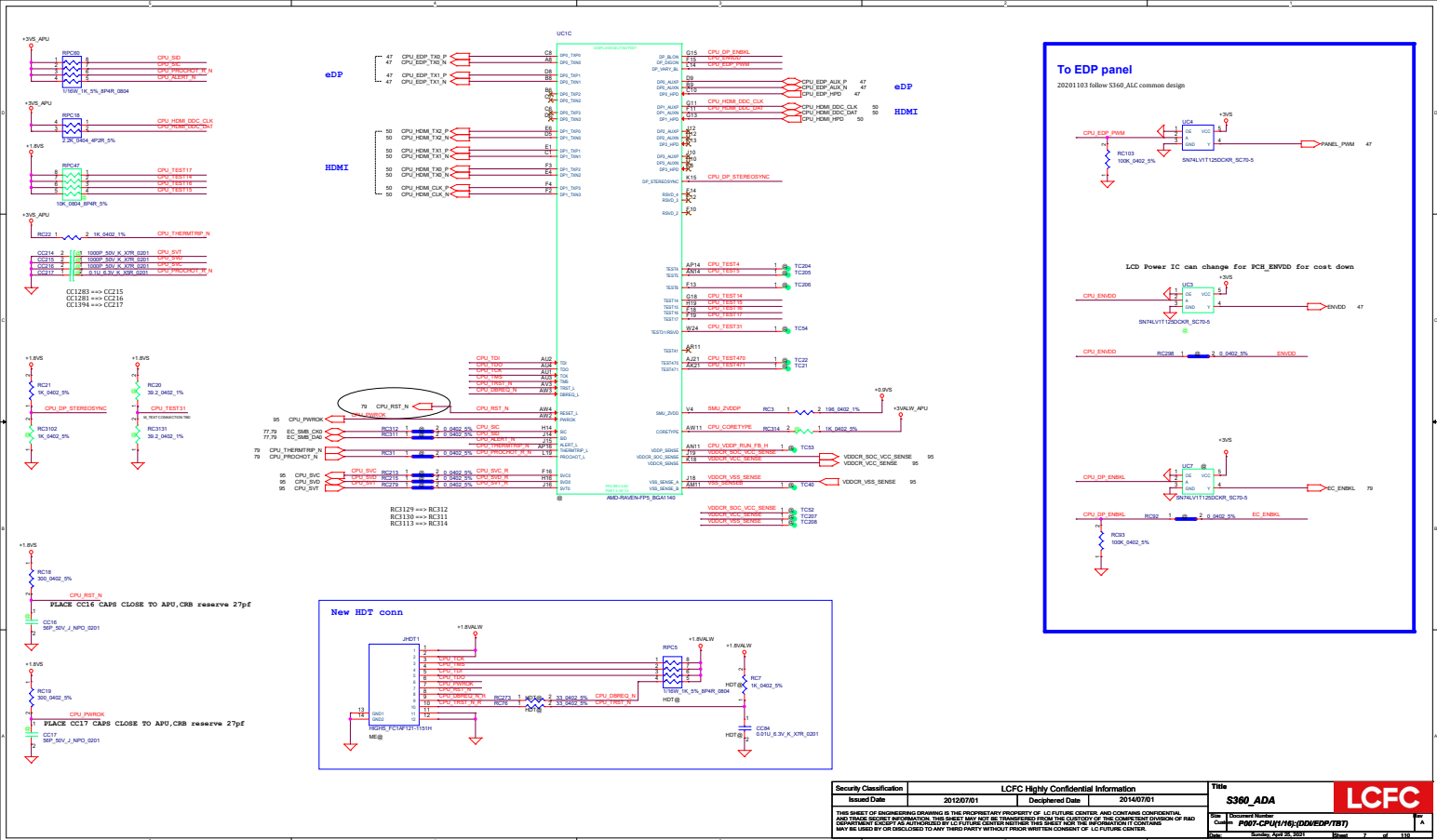
Device	Address
TouchPad	0x15 ELAN
	0x2C Synaptics
	0x38 Focal
	0x2C Cirque

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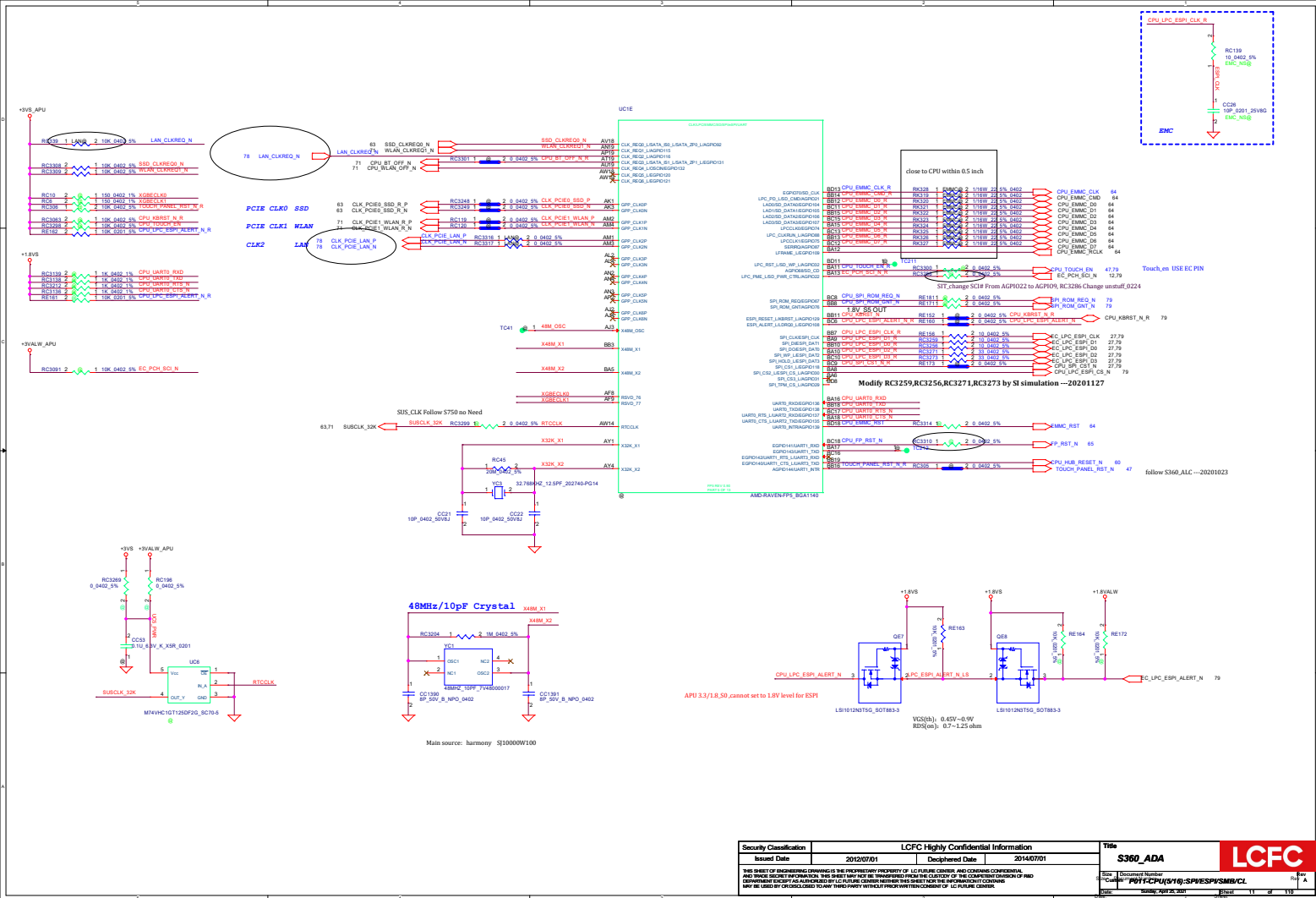
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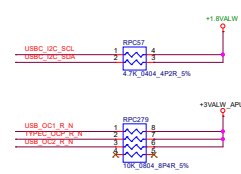
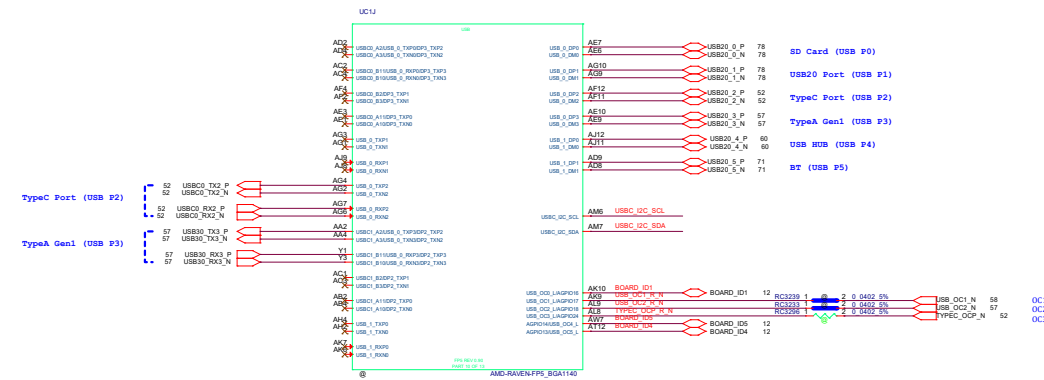
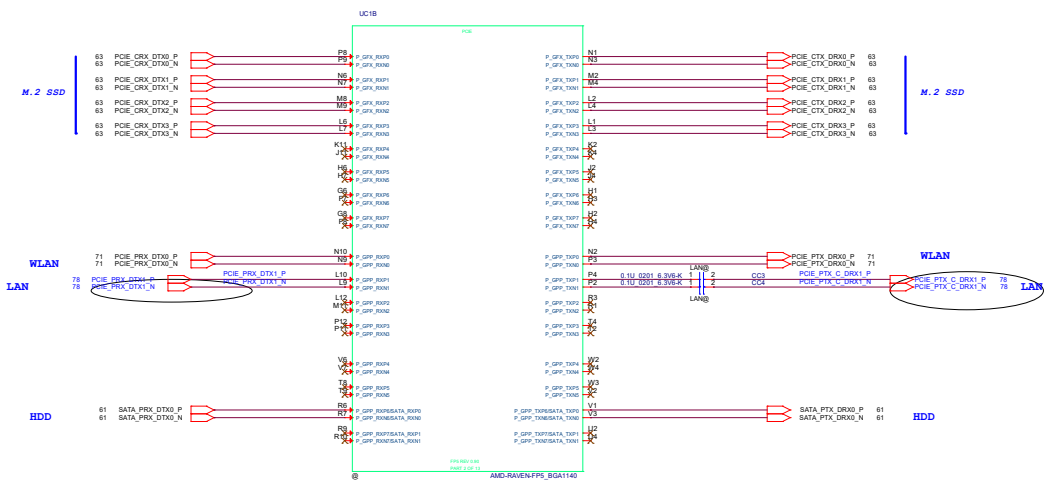


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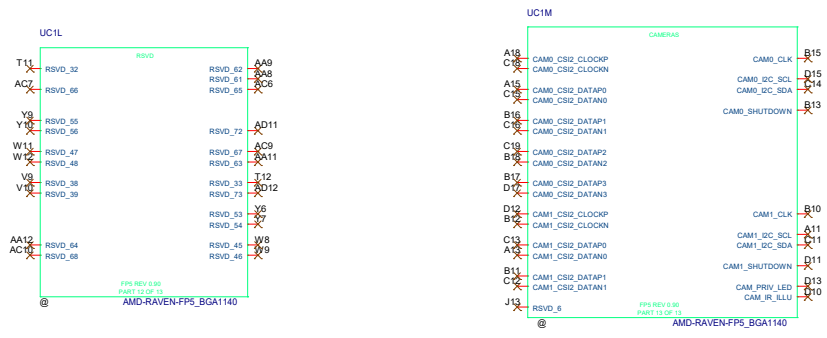


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Doc C	Document Number			P014-CPU(016): PCIE/USB/SATA	
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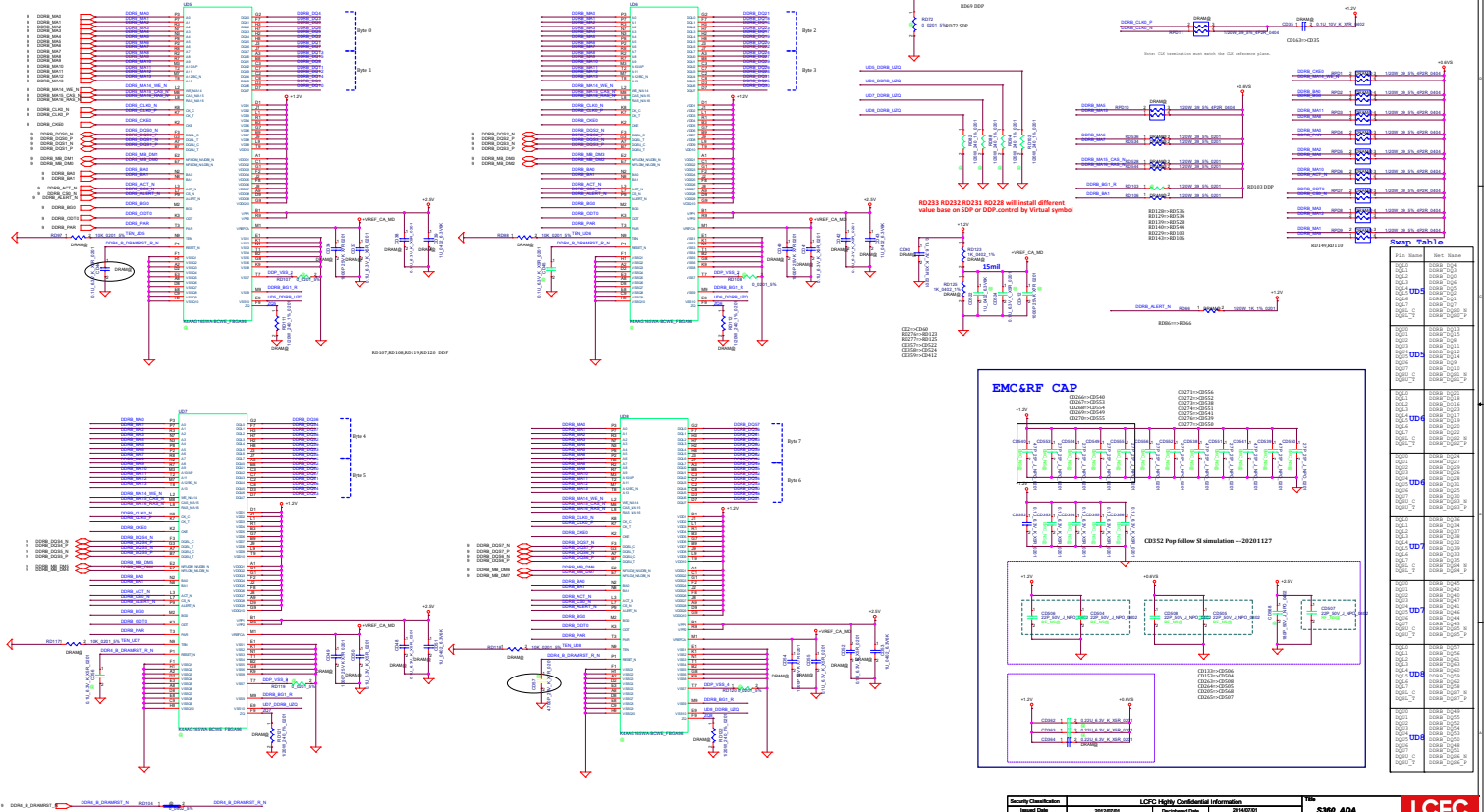


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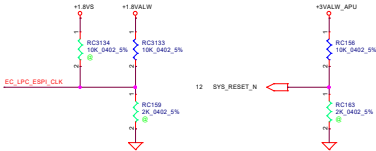
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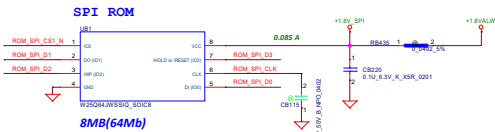
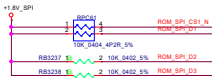


STRAP PINS



STRAP PINS	SYS_RESET#
PCH_SPI_CLK	1:USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS(DEFAULT) 0:USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
SYS_RESET#	1:NORMAL RESET MODE(DEFAULT) 0:SHORT RESET MODE

SPI ROM



ROM_SPI_CS1_N	RC3254	1	2	0 10K 0402 5%	ZPU_SPI_CS1_N	11.79
ROM_SPI_CLK	RE155	1	2	0 10K 0402 5%	EC_LPC_ESPI_CLK	11.79
ROM_SPI_D0	RC3255	1	2	0 10K 0402 5%	EC_LPC_ESPI_D0	11.79
ROM_SPI_D1	RC3256	1	2	0 10K 0402 5%	EC_LPC_ESPI_D1	11.79
ROM_SPI_D2	RC3257	1	2	0 10K 0402 5%	EC_LPC_ESPI_D2	11.79
ROM_SPI_D3	RC3258	1	2	0 10K 0402 5%	EC_LPC_ESPI_D3	11.79

Modify RE155,RC3255,RC3256,RC3257,RC3258 by SI simulation --20201127

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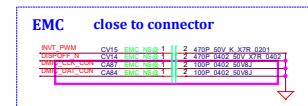
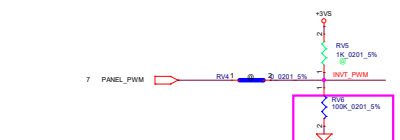
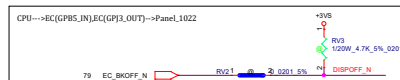
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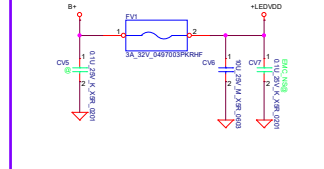
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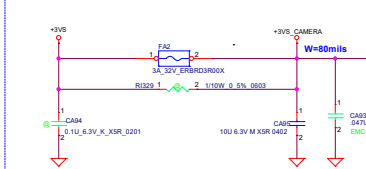
LCD Power Circuit Follow Intel S360ITL_0610



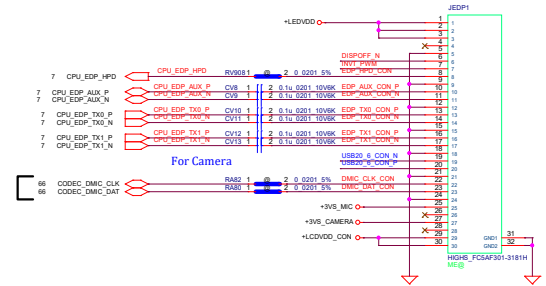
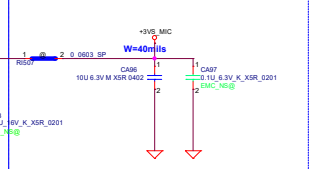
LED Power Follow Intel S360ITL_0610



Camera

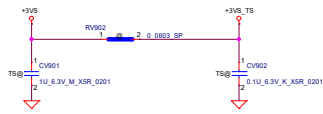


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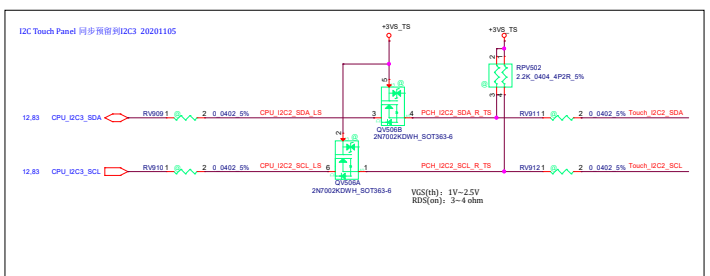
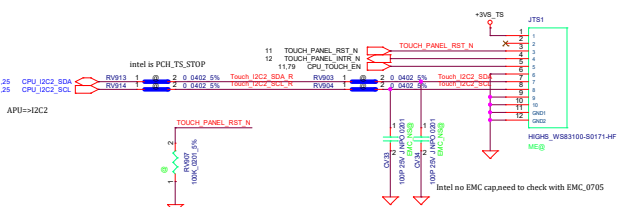



Touch Screen

Touch Panel Power_Follow s750_0705



confirm Pin define with ME



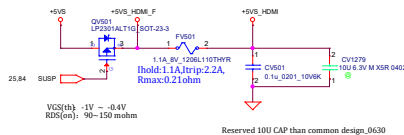
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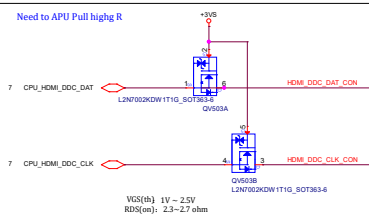
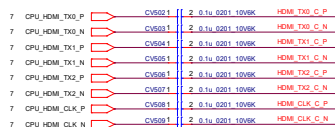
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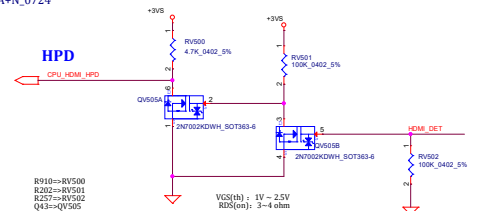
HDMI Power



Reserved 10U CAP than common design 0630

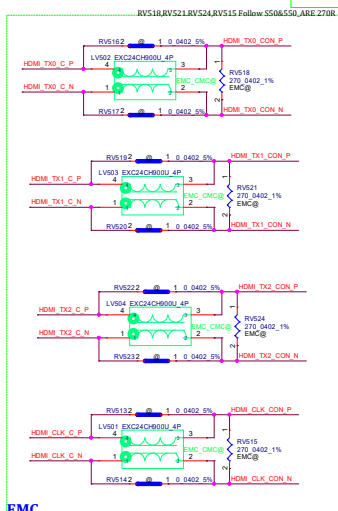


VGS(th): 1V ~ 2.5V
RDS(on): 2.3~2.7 ohm

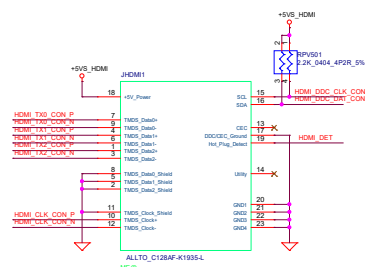


R910=>RV500
R202=>RV501
R257=>RV502
Q43=>QV505

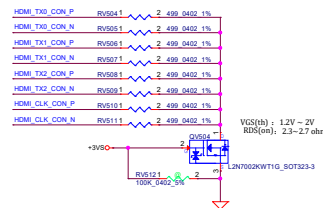
VGS(th) : 1V ~ 2.5V
RDS(on): 3~4 ohm



EMC

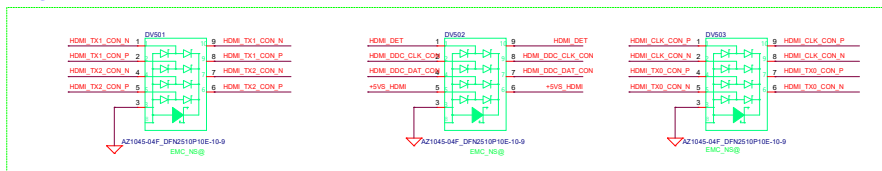


common desing: Rtmds 470R, On CAP with Common choke_0630




VGS(th) : 1.2V ~ 2V
RDS(on) : 23~27 ohm

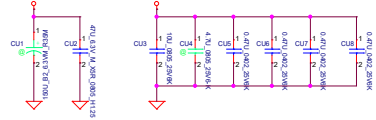
EMC



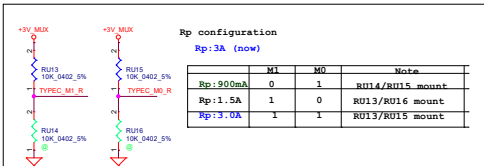
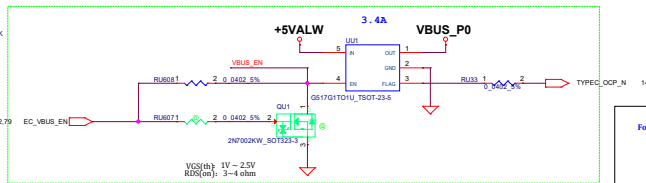
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+5VALW



20201009 Add follow S360 SLC
change R234 9R to 10K
ADD EC control Power Output



Rp configuration

Rp:3A (now)

	R1	R2	Note
Rp:900mA	0	1	R014/R015 mount
Rp:1.5A	1	0	R013/R016 mount
Rp:3.0A	1	1	R013/R015 mount



For C.VBUS
power switch enable pin

Power switch enable pin	Note
Low Active	R017 mount
High Active	R018 mount

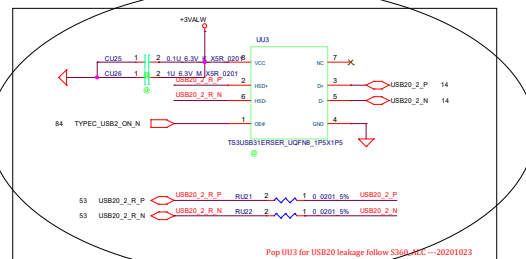
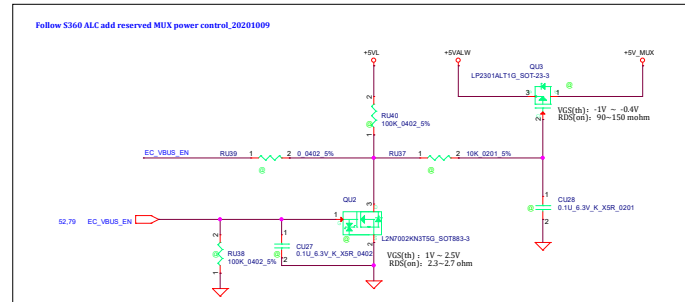
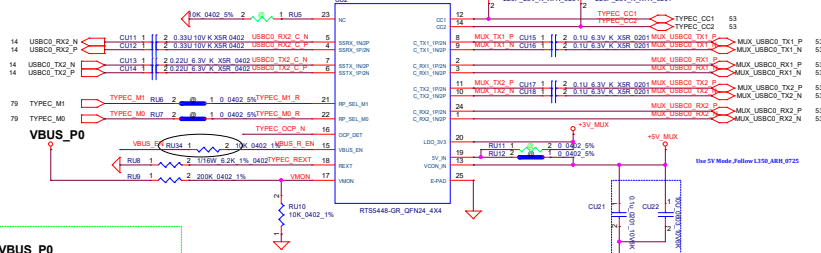


PU AT CPU side 0711

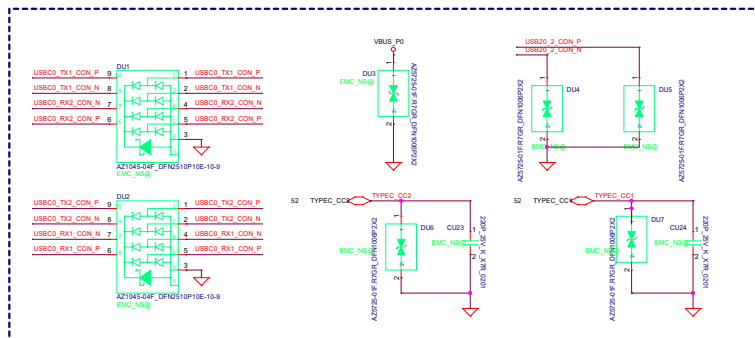
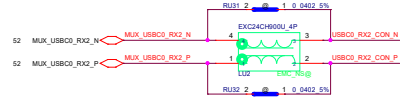
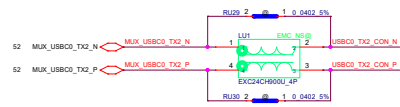
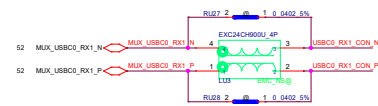
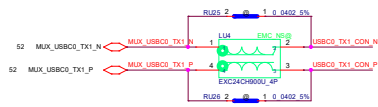
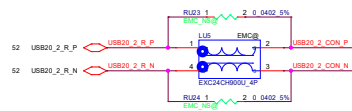
For C.VBUS
power switch OCP pin

Power switch OCP pin	Note
Low Active	R019 mount
High Active	R020 mount

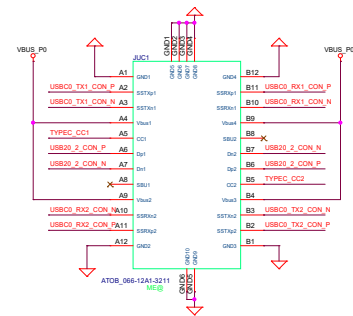
change R019 unstuff to stuff for solve DC SS to S0 U DISK LOSS 20210104



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Issue	2015.04.25.2011	Issue	52	of 110



EMC Require stuff on frist phase, SDV output report Removes==>0804



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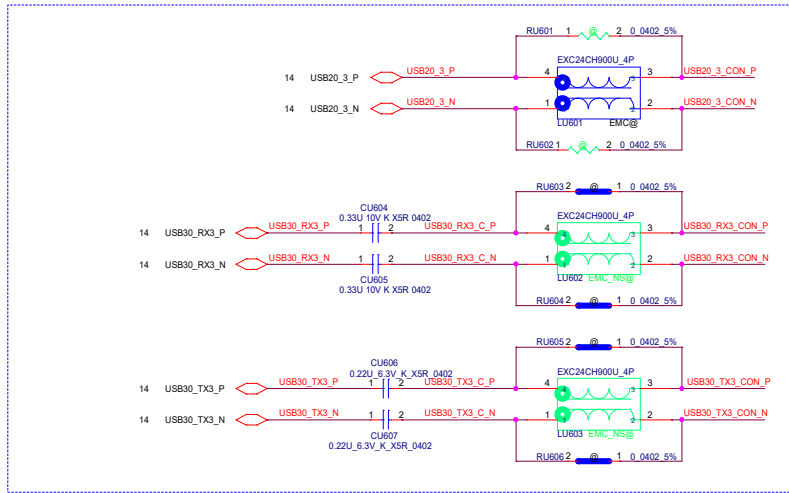
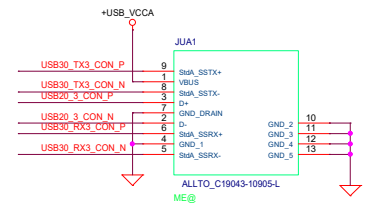
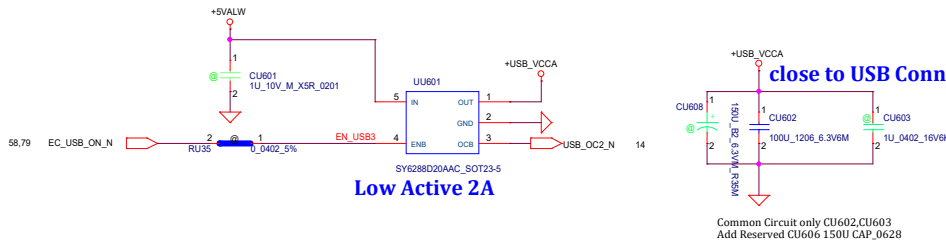
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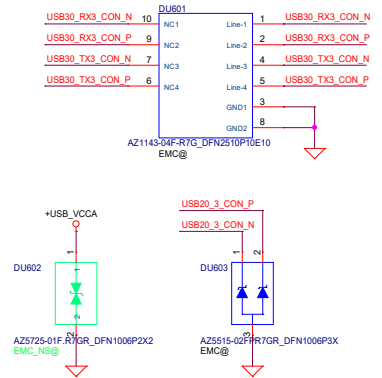


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<small>Issue Date: Sunday, April 25, 2021</small>				Sheet 56 of 119

USB3.0 PORT



EMC close to USB Conn

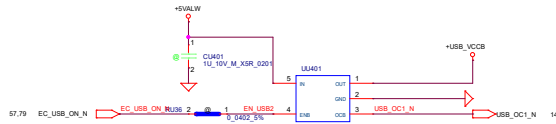


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USB2.0 Port and CMC&TVS&CAP MOVE to SUB Board


USB2.0 PORT



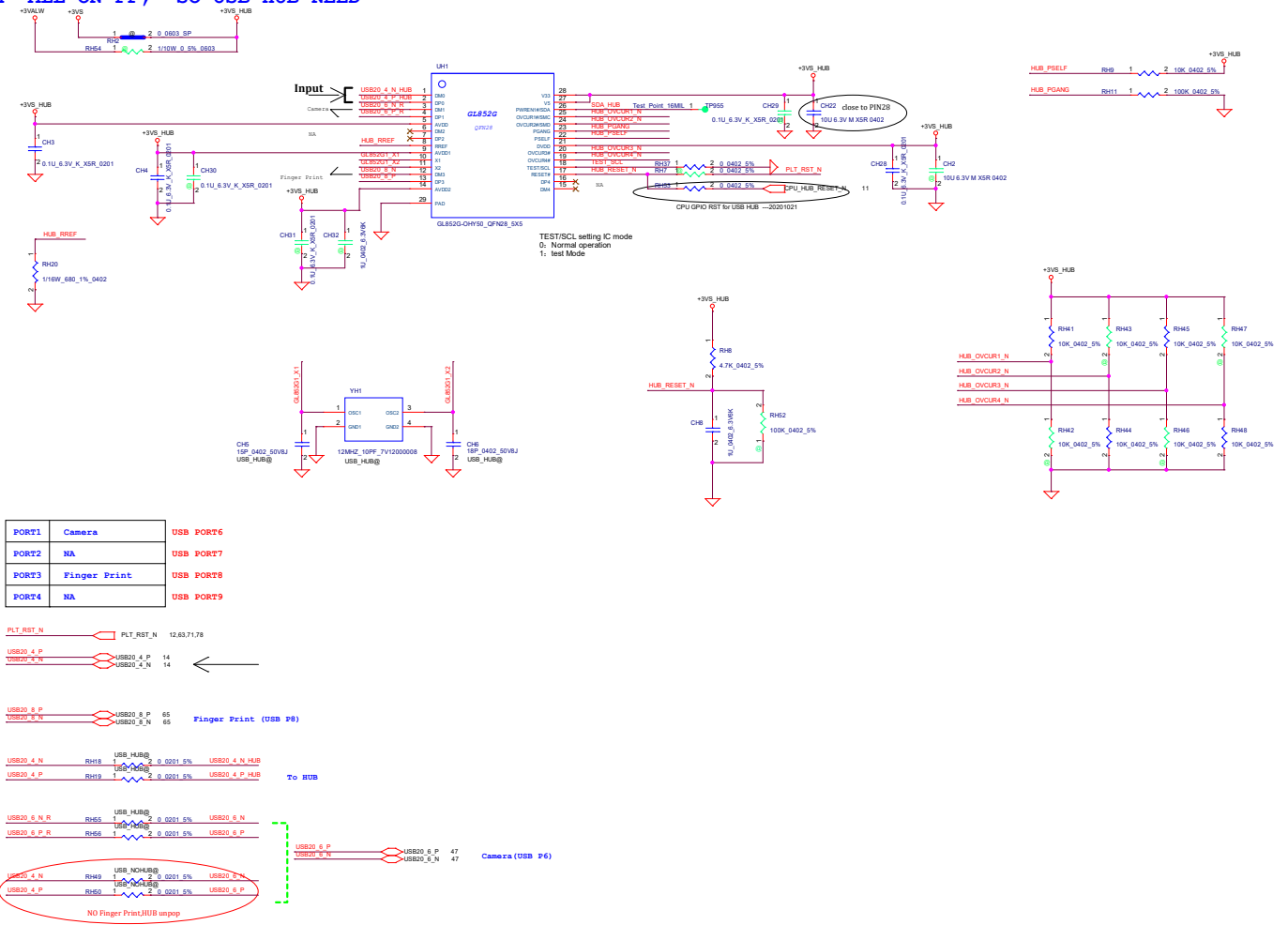
Low Active 2A

the diffrent with Base:
1.S540 No USB2.0 only,S360&V14V15 have

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USB Hub
S360_ADA



PORT1	Camera	USB PORT6
PORT2	NA	USB PORT7
PORT3	Finger Print	USB PORT8
PORT4	NA	USB PORT9

PLT_RST_N PLT_RST_N 12,63,71,78

USB20_4_P 14
USB20_4_N 14

USB20_8_P		USB20_8_P	65
USB20_8_N		USB20_8_N	65

USB20_4_N RH18 1 USB_HUB 2 0 0201 5% USB20_4_N_HUB
USB20_4_P RH19 1 USB_HUB 2 0 0201 5% USB20_4_P_HUB

USB20_6_N R RH55 1 2 0 0201 5% USB20_6_N

USB20_6_P R RH56 1 2 0 0201 5% USB20_6_P

USB20_4_N RH49 1 2 0 0201 5% USB20_6_N

USB20_4_P RH50 1 2 0 0201 5% USB20_6_P

NO Finger Print,HUB unpop

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Size		C		Document Number		P860-USB HUB		Rev A	
Date		April 25, 2012		Sheet		66		of 110	


14.61	SATA_PTX_DRXD_0	P	SATA_PTX_DRXD_0	RK1	0.0201%	CS0	SATA_PTX_DRXD_0	SATA_PTX_DRXD_0	2.0 0.10 4.3V x 7K7 0201	SATA_PTX_DRXD_CON_P
				SATA_HREQ_1			SATA_HREQ_0			
14.61	SATA_PTX_DRXD_0	N	SATA_PTX_DRXD_0	RK2	0.0201%	CS0	SATA_PTX_DRXD_0	SATA_PTX_DRXD_0	2.0 0.10 4.3V x 7K7 0201	SATA_PTX_DRXD_CON_N
				SATA_HREQ_1			SATA_HREQ_0			
14.61	SATA_PRX_DRXD_0	P	SATA_PRX_DRXD_0	RK3	0.0201%	CK10	SATA_PRX_DRXD_0	SATA_PRX_DRXD_0	2.0 0.10 4.3V x 7K7 0201	SATA_PRX_DRXD_CON_P
				SATA_HREQ_1			SATA_HREQ_0			
14.61	SATA_PRX_DRXD_0	N	SATA_PRX_DRXD_0	RK4	0.0201%	CK11	SATA_PRX_DRXD_0	SATA_PRX_DRXD_0	2.0 0.10 4.3V x 7K7 0201	SATA_PRX_DRXD_CON_N
				SATA_HREQ_1			SATA_HREQ_0			

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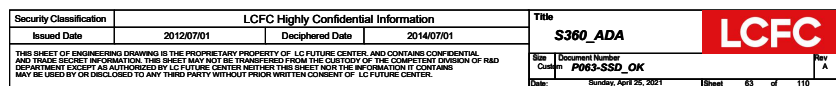
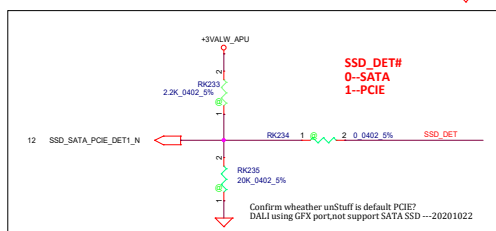
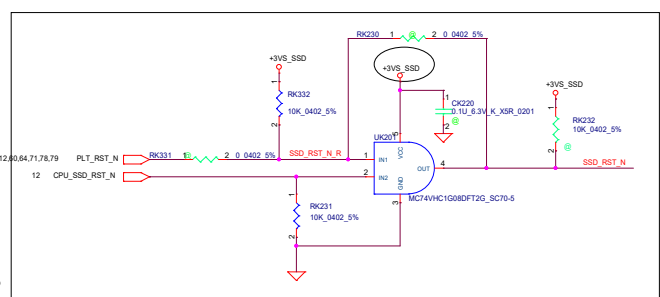
REXT: external res for output swing adjustment
it can be left open or tie to GND, internally generated bias
current be used and the output is as default swing setting;

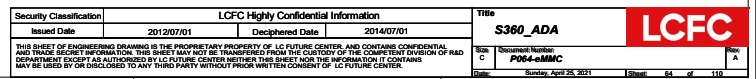
the pin can be connected 4.99k to GND, the output swing
will be at the default value with Reference to the ex RES

DEW: De-emphasis width setting for A&B

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				Rev	A
P062-Blank				LCFC	
Date				Smiley, April 25, 2011	Sheet 92 of 110





FP Power Control

FP Power Control

VGS(th): -1V ~ -0.4V
RDS(on): 90~150 mohm

3VL

Q13 LP2301ALT1G_SOT-23-3

1FPR_PWR_OUT

R15 1 0402_5%

2 0

FP_PWR

0.1uF_0201_5%K

C12

FP@

1 2

2 1

20p0 45X M K 5.6 3 101

3VL

1/20W_200K_5%_0201

R12

FP@

2 1

1 2

0.047uF_0402_16V_X7R

C1

FP@

2 1

1 2

0.1uF_6.3V_K_X5R_0201

C3

2 1

1 2

0.1uF_6.3V_K_X5R_0201

C4

2 1

1 2

0.1uF_0201_5%

C5

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C6

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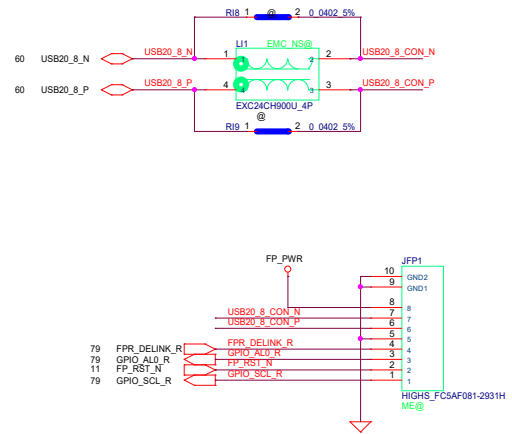
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C79

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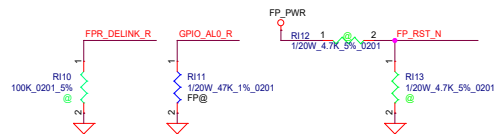
close to Conn


The diagram illustrates the wiring for the USB2.0 connector. The USB2.0 pins are connected to the board components as follows:

- USB2_0_CON_N (Pin 1) connects to FPR_DELINK_R0 (Pin 1).
- USB2_0_CON_P (Pin 2) connects to GPIO_AL0_R (Pin 2).
- D+ (Pin 3) connects to FP_RST_N (Pin 3).
- D- (Pin 4) connects to GPIO_SCL_R (Pin 4).
- GND1 (Pin 5) connects to GND1 (Pin 5).
- GND2 (Pin 6) connects to GND2 (Pin 6).

The board components are also connected to each other:

- FPR_DELINK_R0 (Pin 1) connects to GPIO_AL0_R (Pin 2).
- GPIO_AL0_R (Pin 2) connects to FP_RST_N (Pin 3).
- FP_RST_N (Pin 3) connects to GPIO_SCL_R (Pin 4).
- GPIO_SCL_R (Pin 4) connects to GND1 (Pin 5).
- GND1 (Pin 5) connects to GND2 (Pin 6).
- GND2 (Pin 6) connects to GND1 (Pin 5).

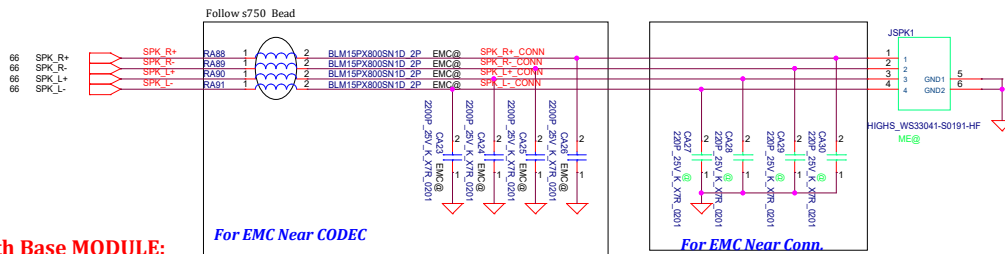


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Date				Sheet	of



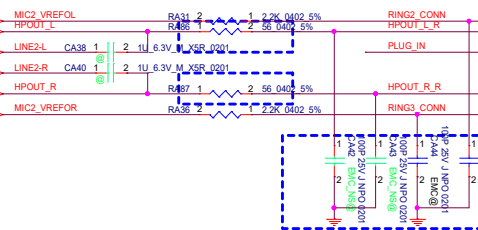
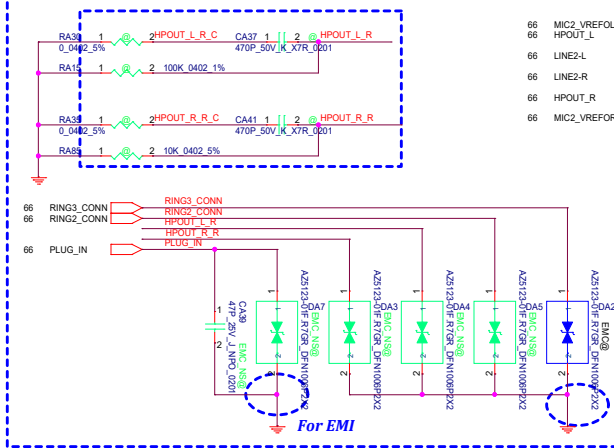


the different with Base MODULE:
 1.S360&V14&V15 RA86&RA87 VALUE different with module,

2.for EMC TVS EMC_NS@ type different with module

3.GND type different

4.module no CA37&CA41 part circuit,S360&V14&V15 reserve



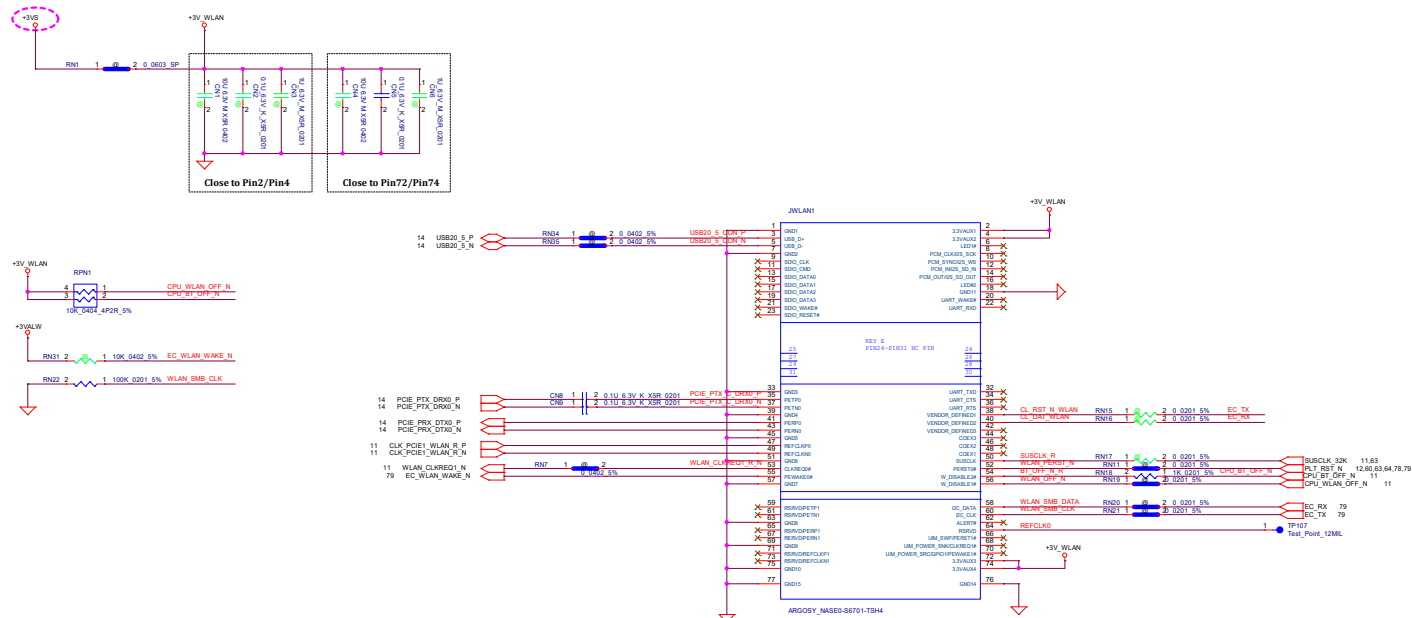
Conector list USE 063-RT04-0701


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Date:	Sunday, April 25, 2021		Sheet	69 of 110		A

S360_AUC
Card reader Circuit MOVE to SUB Board S360
USB2.0 on SUB Board

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Date				2015, April 25, 2015	Sheet 78 of 110

Copy Wlan common design



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			Date: <u>Sunday, April 26, 2021</u>	Sheet: <u>71</u> of <u>110</u>

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Date				Sheet	75 of 110

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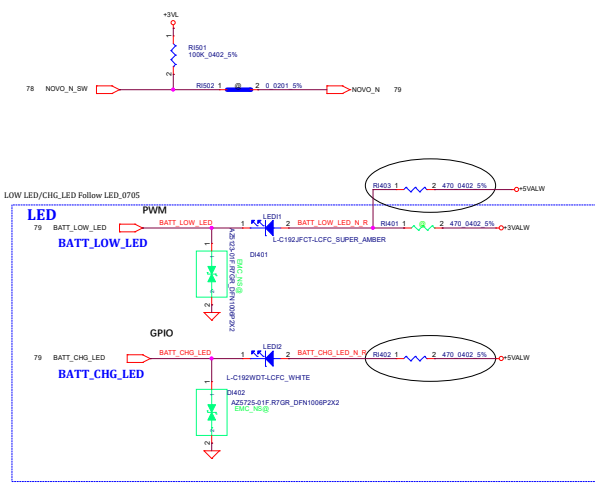
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Size	Document Number				Rev
Custom	P077-Thermal/FAN-S750 OK				A
Date:	Sunday, April 25, 2021		Sheet	77	of 110

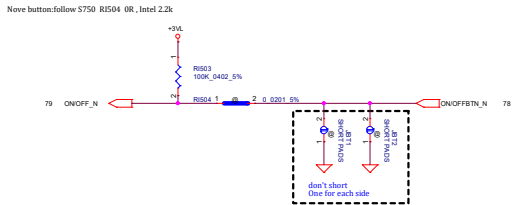
Title		S360_ADA		LCFC	
Size	Document Number				Rev
C	P078-Sub Board CONN_Only 36PIN				A
Date:	Sunday, April 25, 2021	Sheet	78	of	110

NOVO BUTTON



Power LED
check S750_ARH IO Board_0705

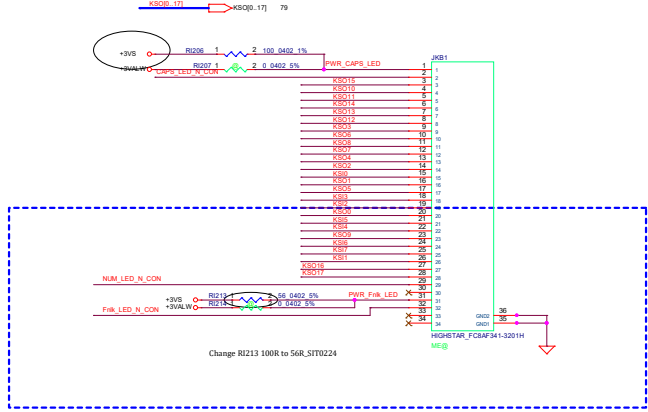
PWR BUTTON



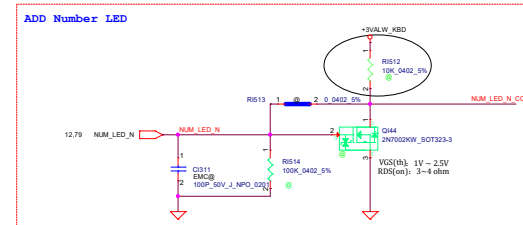
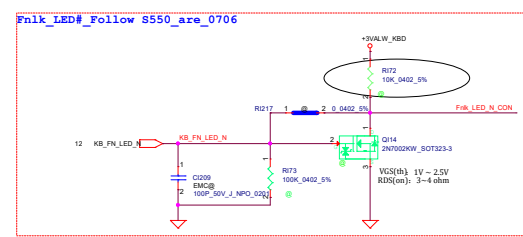
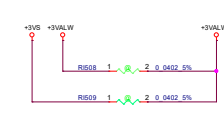
LED		LED Behavior	
State (Same as the power button LED)	State	LED Behavior	
	System on	White on (battery 211-1001)	
	Standby LED closed	White on, 500ms off (battery 01-201)	
	System off	off	
Charging	Battery only	off	
	Charging	White on (battery 111-1001)	

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				P080-LED/Buttons	A
				Issue	Sheet
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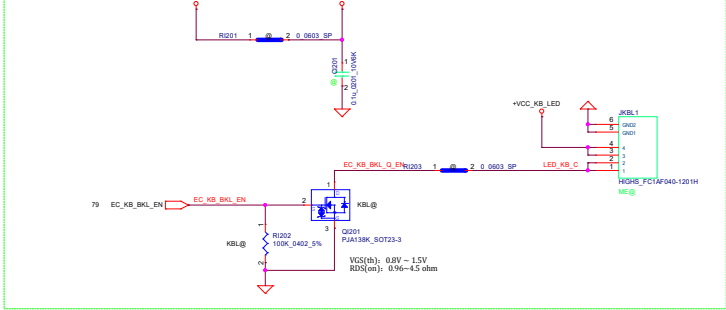
K/B Connector



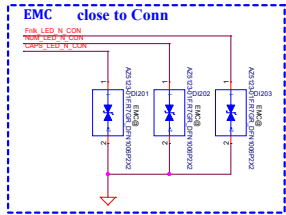
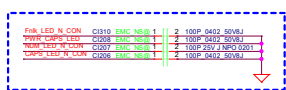
K/B Connector



KB Backlight Connector



the diffrent with module:
1.modulel No 15 KB,S360&V14V15 have



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				P081-KB/KBL_CONN_Intel	A
				Sheet	81 of 110

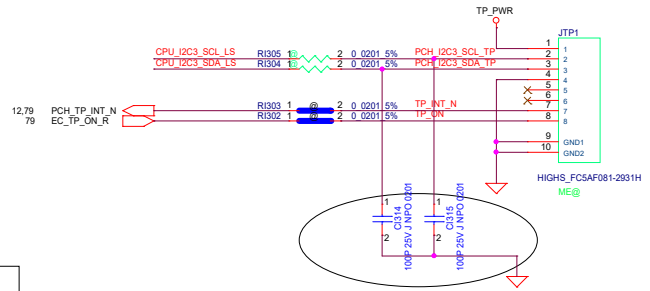
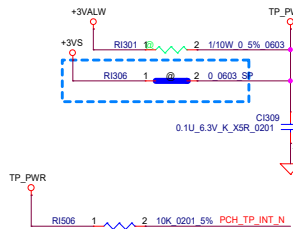
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				P082-Blank	A
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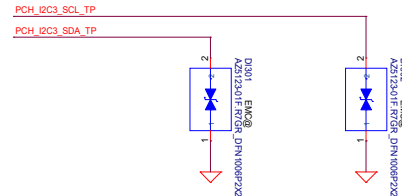
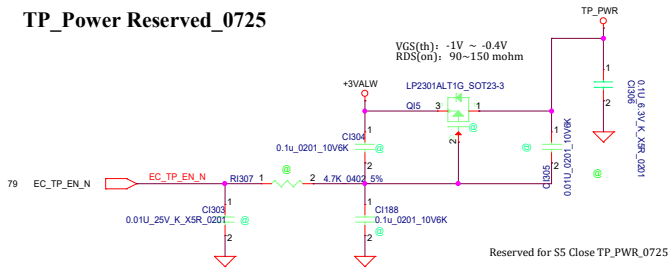
Touch Pad

Need support wake up by touch pad
Follow latest UE spec

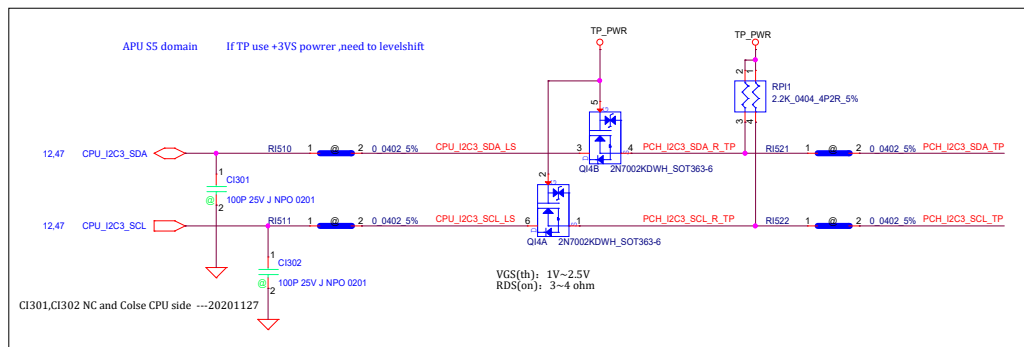
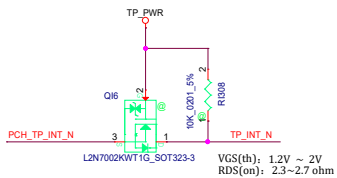
(the different with Base MODULE:
1.Module no RI306,S360&V14&V15 Rerserve) Intel 备注



TP_Power Reserved_0725

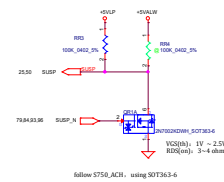
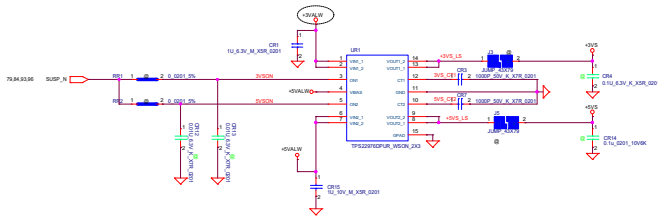


CPU AGPIO89 S0 Power, If TP use S5 PWR Reserve Mosfet_1125

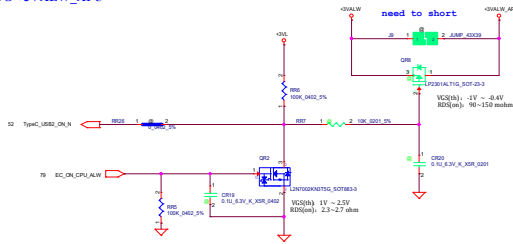


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Size	Document Number				Rev	
Custom	P083-TouchPad CONN_Intel				A	
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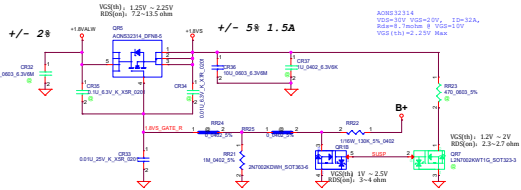
LCFC



TO +3VALW_APU

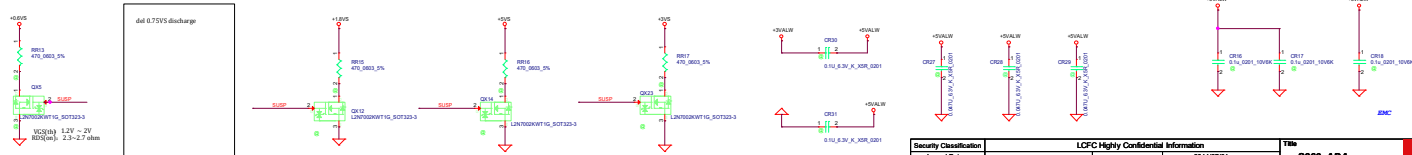


+1.8VALW to +1.8VS



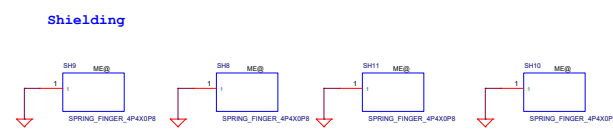
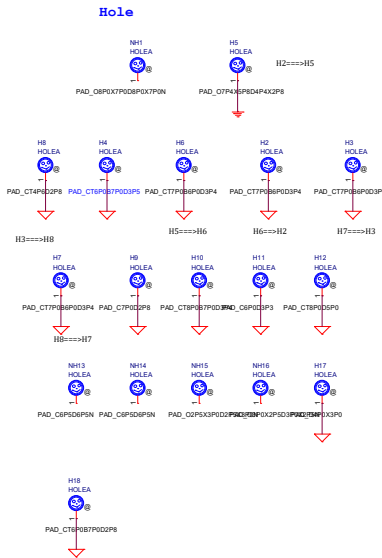
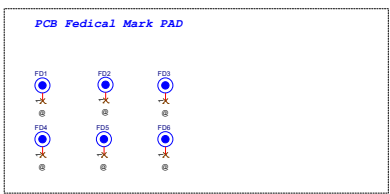
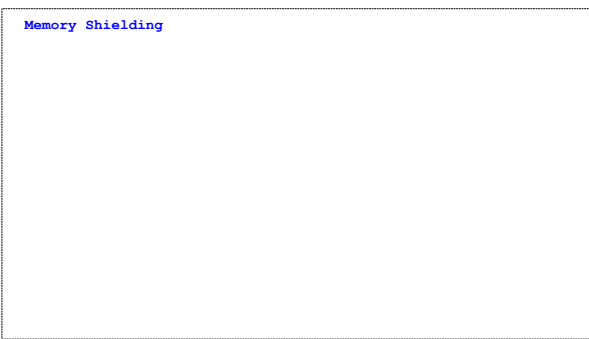
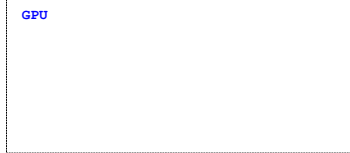
20VSB will change to 6V in DC mode, careful the Res divide voltage

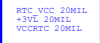
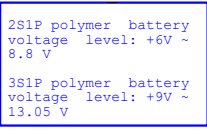
For DisCharge




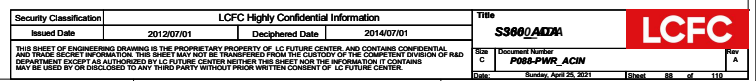
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2012/07/01		2014/07/01		Rev	

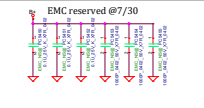
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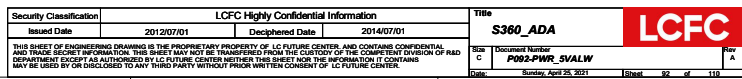
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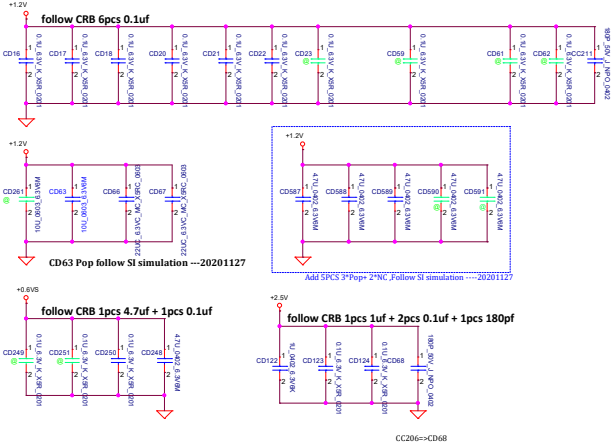


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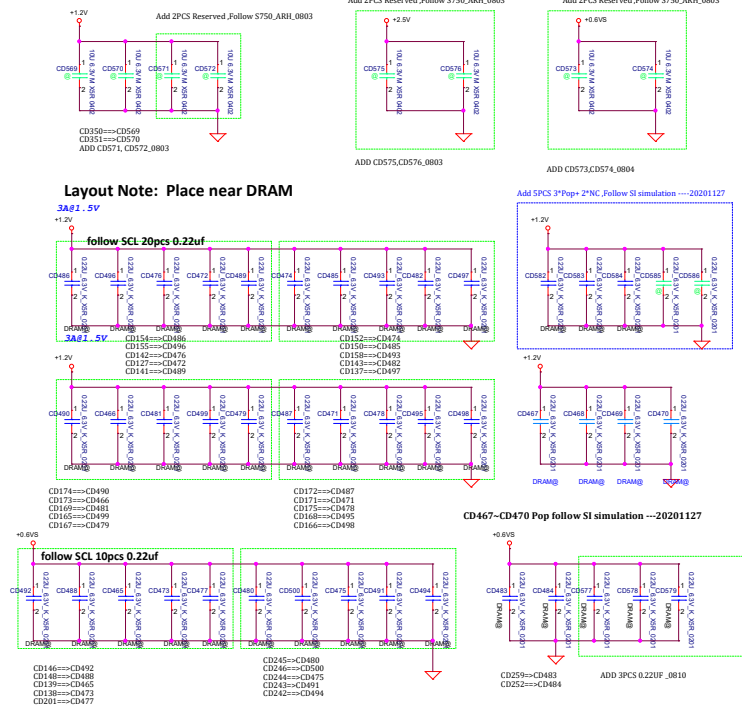
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Doc Number		P090-BLANK					
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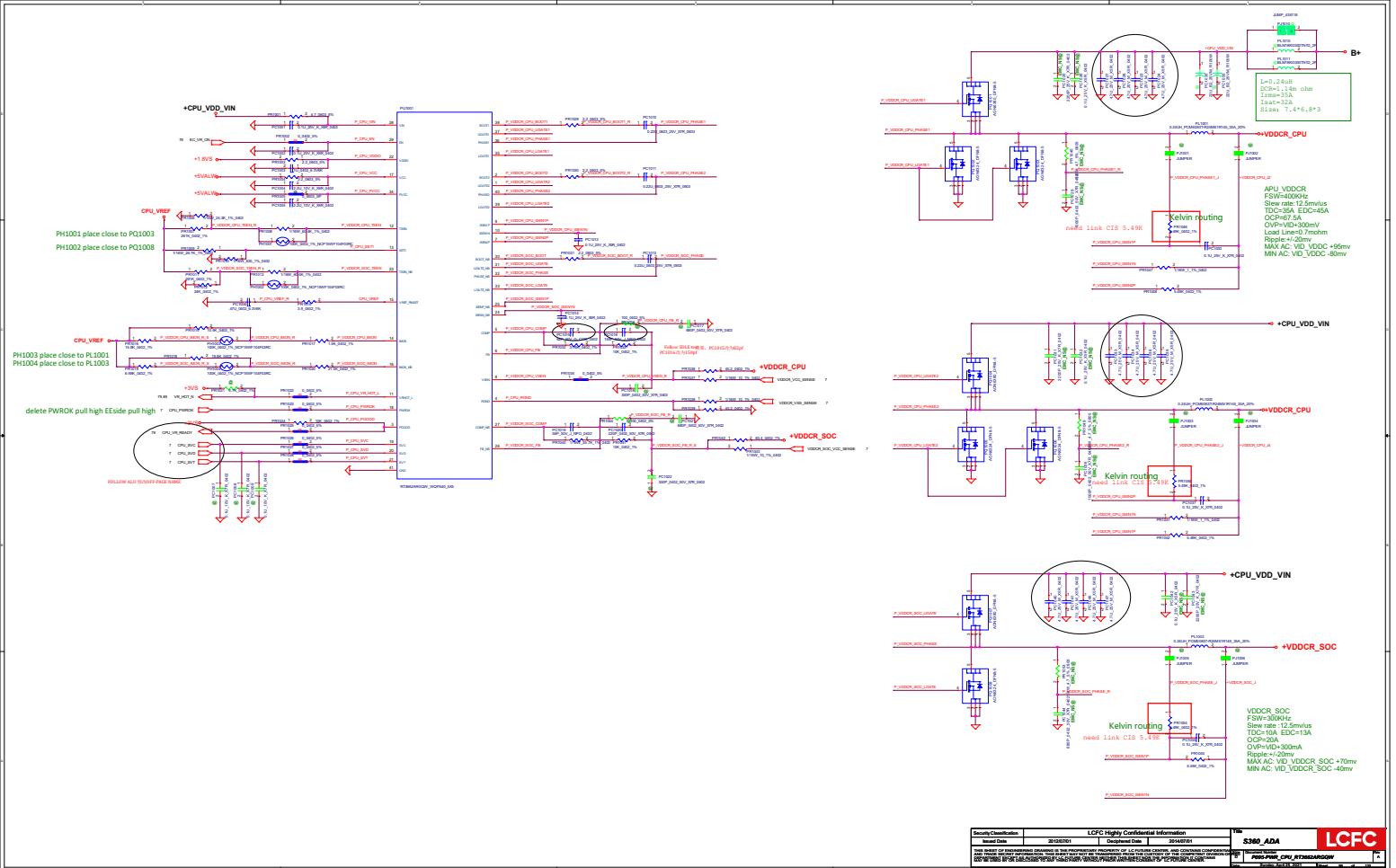
EE Side Channel A SODIMM
Follow S350_ARE_0803

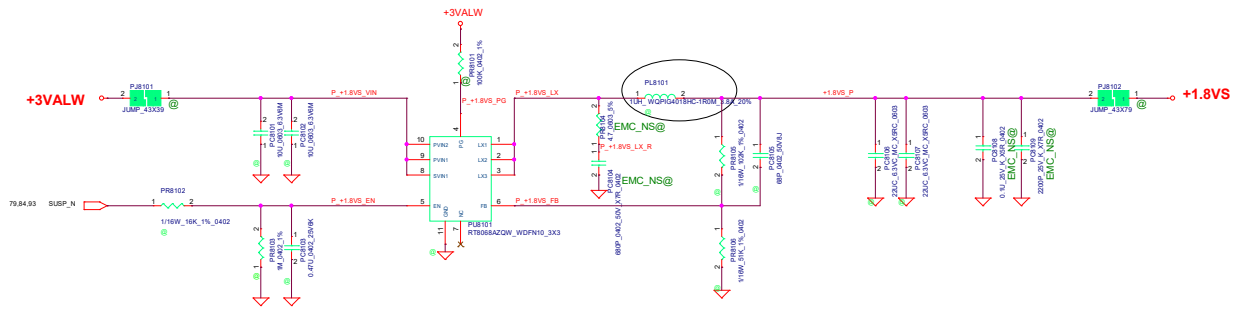


EE Side Channel B MD



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				P084-PWR_Memory Decoupling	A
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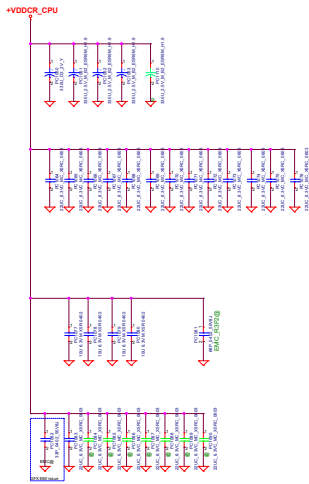


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				P086-PWR_1.8VS_R78088AZQW	A
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				P007-BLANK	A
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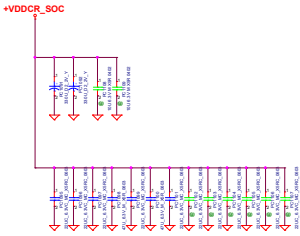
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Output CAP:330u/9m D2*4+22uF*14+10u-0402*4
FD: 22u+3PCS 10u+3PCS

Under the processor

VDDCR	330u D2	22u	10u	100p
PDG		16		1
S350_ADA	4	13	4	1
S360_ADA	4 + 1* NC	14	4	1



Output CAP:330u/9m D2*2+22uF*7

Follow SDLE test 结果, PC1098 和PC1100改为47uf
2021/02/26

Under the processor

VDDCR_SOC	330u D2	22u	10u	1u	100p
PDG		7		1	1
S350_ADA	4	7+6* NC	2+2* NC		
S360_ADA	2	7+6* NC	2+2* NC		

5	4	3	2	1																													
D				D																													
C				C																													
B				B																													
A				A																													
<table><tr><td>Security Classification</td><td colspan="3">LCFC Highly Confidential Information</td><td>Title</td><td colspan="2">S360_ADA</td><td rowspan="2">LCFC</td></tr><tr><td>Issued Date</td><td>2012/07/01</td><td>Deciphered Date</td><td>2014/07/01</td><td>Size</td><td>Document Number</td><td>Rev</td></tr><tr><td colspan="4">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</td><td>B</td><td>P099-BLANK</td><td>A</td></tr><tr><td colspan="4"></td><td>Date:</td><td>Sunday, April 25, 2021</td><td>Sheet 99 of 110</td></tr></table>					Security Classification	LCFC Highly Confidential Information			Title	S360_ADA		LCFC	Issued Date	2012/07/01	Deciphered Date	2014/07/01	Size	Document Number	Rev	THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				B	P099-BLANK	A					Date:	Sunday, April 25, 2021	Sheet 99 of 110
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				Date:	Sunday, April 25, 2021	Sheet 99 of 110																											
5	4	3	2	1																													

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				B	P104-BLANK	A
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